adjusting means for controlling said delaying means so that, when said phase of said predetermined rising edge is judged to be behind said phase of said first rising edge by said phase-detecting means, said delaying means delays said phase of said output second periodic signal until said phase of said predetermined rising edge and a phase of a second rising edge of said input first periodic signal match each other, the second rising edge being one period behind said first rising edge, wherein the delaying, phase-detecting and adjusting is irrespective of the comparison during an initiation period.

Cont'd A3

A copy of the marked up amended claims is attached to this response showing the changes as set forth in amended 37 C.F.R. § 1.121.

REMARKS

Claims 1-8 are pending in this application. By this Amendment, claims 1 and 3-7 are amended. Support for the Amendment is found in the specification. No new matter is added. This Response is submitted as a full and complete response to the outstanding Office Action.

MATTERS OF FORM

The Office Action objects to the drawings, particularly, for a misspelled word. Applicant has corrected the misspelled word in Fig. 5 according to the attached Request for Approval of Drawing Corrections. Upon approval of the Request, formal drawings will be timely filed. Accordingly, Applicant respectfully requests the withdrawal of the objection to the drawings.

The Office Action objects to the specification for a typographical error. Applicant has amended the specification to obviate this rejection. Accordingly, Applicant respectfully requests the withdrawal of the objection to the specification.

CLAIMS 1-8 CONTAIN PATENTABLE SUBJECT MATTER

The Office Action rejects claims 1-8 under 35 U.S.C. §102(e) over Lu (U.S. Patent No. 6,100,735). Applicant respectfully submits that claims 1-8 contain subject matter neither disclosed nor suggested in this cited art.

Specifically, Applicant's independent claim 1 recites a delay time adjusting method of adjusting a delay time of an input signal so that a phase of said input signal and a phase of an output signal match each other, based on a comparison between phases of said input signal and said output signal. The method having the steps of delaying said phase of said output signal irrespective of said comparison during an initiation period.

Applicant's independent claim 3 recites a delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal. The method comprises the step of adjusting the delay time so that, when a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a predetermined rising edge of the input first periodic signal, the predetermined rising edge of the output second periodic signal matches a rising edge of the input first periodic signal, wherein a phase of the rising edge is behind and nearest to the phase of the predetermined rising edge of the output second periodic signal,

wherein the adjusting of said delay is irrespective of said comparison during an initiation period.

Applicant's independent claim 4 recites a delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal. The method comprising a first step of judging whether a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a first rising edge of the input first periodic signal, and a second step of delaying the phase of the output second periodic signal so that, when the phase of the predetermined rising edge is judged to be behind the phase of said first rising edge in the first step, the phase of the predetermined rising edge and a phase of a second rising edge of the input first periodic signal match each other. The second rising edge is one period behind the first rising edge, wherein the judging and delaying is irrespective of the comparison during an initiation period.

Applicant's independent claim 5 recites a delay time adjusting circuit for adjusting a delay time of an input signal so that a phase of the input signal and a phase of an output signal match each other between phases based on a comparison of the input signal and the output signal. The circuit comprises detecting means for detecting a phase difference between the phase of said input signal and the phase of said output signal, and delaying means for delaying the phase of the output signal until the phase difference becomes N periods, where N is an integer other than zero.

Applicant's independent claim 6 recites a delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal. The circuit comprises judging means for judging whether a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a predetermined rising edge of the input first periodic signal, and a delaying means for adjusting the delay time so that, when the phase of said predetermined rising edge of the output second periodic signal is judged to be behind the phase of said predetermined rising edge of the input first periodic signal by said judging means, the predetermined rising edge of said output second periodic signal matches a rising edge of the input first periodic signal. A phase of the rising edge is behind and nearest to the phase of the predetermined rising edge of the output second periodic signal, wherein the judging and delaying is irrespective of the comparison during an initiation period.

Applicant's independent claim 7 recites a delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal. The circuit comprises delaying means for delaying said input first periodic signal so as to generate the output second periodic signal, a phase-detecting means for detecting whether a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a first rising edge of the input first periodic signal. The circuit also includes an adjusting means for controlling the delaying means

so that, when the phase of the predetermined rising edge is judged to be behind the phase of the first rising edge by the phase-detecting means, the delaying means delays the phase of the output second periodic signal until the phase of the predetermined rising edge and a phase of a second rising edge of the input first periodic signal match each other. The second rising edge is one period behind the first rising edge, wherein the delaying, phase-detecting and adjusting is irrespective of the comparison during an initiation period.

Lu discloses a delay time adjusting method, which is similar to a Rambus method. In the Rambus method, phases within 360 degrees are prepared, and a pair of phases are selected so that a desired phase is located therebetween. An optimum phase is further selected between the pair of phases by dividing the interval between the pair of phases. However, there is a problem in the delay time adjusting method of Lu in that when the operation goes into an underflow state, the delay time in the DLL array cannot be adjusted due to the phase of a delay clock signal being behind the phase of a target clock signal.

On the other hand, the Applicant's claimed invention specifically addresses the possibility that the operation may go into the underflow state. In the Applicant's delay time adjusting method, a delay is provided irrespective of the initial comparison so as to prevent an occurrence of an underflow state in which a phase of a delay clock signal is behind a phase of a target clock signal of said delay locked loop circuit. Lu does not contain any discussion or suggestion relating to this issue.

In view of the above, Applicant respectfully submit that Lu does not disclose or suggest all of the features of Applicant's claimed invention. Claims 2 and 8 depend

from claims 1 and 7, respectively. Therefore, for at least the above reasons, Applicant respectfully requests the withdrawal of the rejection of claims 1-8 under 35 U.S.C. § 102(e).

CONCLUSION

In view of the above, Applicant respectfully submits that all of claims 1-8 contain patentable subject matter. Favorable consideration and prompt allowance is earnestly solicited.

Should the Examiner believe that anything further is necessary to place the application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicant respectfully petitions for an appropriate extension of time. The Commissioner is authorized to charge

payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300, referring to docket number 100353-00039.

Respectfully submitted,

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JAK:ksm

Enclosure: Marked-Up Copy of Amended Specification
Marked-Up Copy of Amended Claims
Request for Approval of Drawing Corrections
Petition for Extension of Time (one month)

MARKED-UP COPY OF AMENDED SPECIFICATION

Please replace page 11, paragraph 5, starting at line 22 with:

It should be noted that the frequency divider 2 may be considered to be an element that determines a target used in adjusting a phase of a signal. The second frequency divider [12] 4 may be considered to be an element that determines how frequently the phase of a signal has a chance to be adjusted.

MARKED-UP COPY OF AMENDED CLAIMS

1. (Once Amended) A delay time adjusting method of adjusting a delay time of an input signal so that a phase of said input signal and a phase of an output signal match each other, based on a comparison between phases of said input signal and said output signal, the method comprising the [steps] step of:

delaying said phase of said output signal [until a phase difference between said phase of said input signal and said phase of said output signal becomes N period, where N is and integer other than zero] irrespective of said comparison during an initiation period.

3. (Once Amended) A delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of said input first periodic signal and said input second periodic signal, the method comprising the [steps] step of:

adjusting said delay time so that, when a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a predetermined rising edge of said input first periodic signal, said predetermined rising edge of said output second periodic signal matches a rising edge of said input first periodic signal, a phase of the rising edge being behind and nearest to said phase of said predetermined rising edge of said output second periodic signal, wherein the adjusting of said delay is irrespective of said comparison during an initiation period.

4. (Once Amended) A delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a

phase of an output second periodic signal match each other based on a comparison between phases of said input first periodic signal and said input second periodic signal, the method comprising:

a first step of judging whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a first rising edge of said input first periodic signal; and

a second step of delaying said phase of said output second periodic signal so that, when said phase of said predetermined rising edge is judged to be behind said phase of said first rising edge in said first step, said phase of said predetermined rising edge and a phase of a second rising edge of said input first periodic signal march each other, the second rising edge being one period behind said first rising edge, wherein the judging and delaying is irrespective of said comparison during an initiation period.

5. (Once Amended) A delay time adjusting circuit for adjusting a delay time of an input signal so that a phase of said input signal and a phase of an output signal match each other between phases based on a comparison of said input signal and said output signal, the circuit comprising:

detecting means for detecting a phase difference between said phase of said input signal and said phase of said output signal; and

delaying means for delaying said phase of said output signal until said phase difference becomes N periods, where N is an integer other than zero.

6. (Once Amended) A delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a phse of an output second periodic signal match each other based on a comparison between

phases of said input first periodic signal and said input second periodic signal, the circuit comprising:

judging means for judging whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a predetermined rising edge of said input first periodic signal; and

delaying means for adjusting said delay time so that, when said phase of said predetermined rising edge of said output second periodic signal is judged to be behind said phase of said predetermined rising edge of said input first periodic signal by said judging means, said predetermined rising edge of said output second periodic signal matches a rising edge of said input first periodic signal, a phase of the rising edge being behind and nearest to said phase of said predetermined rising edge of said output second periodic signal, wherein the judging and delaying is irrespective of said comparison during an initiation period.

7. (Once Amended) A delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of said input first periodic signal and said input second periodic signal, the circuit comprising:

delaying means for delaying said input first periodic signal so as to generate said output second periodic signal;

phase-detecting means for detecting whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a first rising edge of said input first periodic signal; and

adjusting means for controlling said delaying means so that, when said phase of said predetermined rising edge is judged to be behind said phase of said first rising edge by said phase-detecting means, said delaying means delays said phase of said output second periodic signal until said phase of said predetermined rising edge and a phase of a second rising edge of said input first periodic signal match each other, the second rising edge being one period behind said first rising edge, wherein the delaying, phase-detecting and adjusting is irrespective of the comparison during an initiation period.